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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/813,124	03/31/2004	Jerzy A. Teterwak	100628.53197US	3711

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EXAMINER	
JEANGLAUDE, JEAN BRUNER	
ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 10/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/813,124	TETERWAK, JERZY A.	
	Examiner	Art Unit	
	Jean B Jeanglaude	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,11-17 and 21-40* is/are rejected.

7)☒ Claim(s) *8-10 and 18-20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 March 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

Drawings

Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.121(d)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1 – 7, 11 – 17, 21 – 26, 28 - 40 are rejected under 35 U.S.C. 102(b) as being anticipated by Watson (US patent Number 6,445,322).

3. Regarding claims 1, 24, 28, 40, Watson discloses a current steering digital-to-analog (DAC) and method (figs. 1a – 2), comprising: a plurality of current steering segments (101-1,..., 101-n) each comprising differential transistors to steer a current from a summing node to either a positive output or a negative output of the DAC (col 2, lines 6 – 15); and a control circuit to reduce a variation of a voltage present at the

summing node of each of the current steering segments (col 1, lines 24 – 34) [note that it is indicated that each of the current cell shown in fig. 1 comprises a control terminal that is used to control the differential input stage of the current cell, thereby in controlling the differential input stage of the cell the control circuit is reducing the variation in the voltage present at the summing node in response to the output].

4. Regarding claims 2, 29, 31, 32, 34, Watson discloses a current steering DAC and method (figs. 1a – 2) wherein the control circuit comprises a first control circuit to reduce the variation of the voltage present at the summing node of each of the current steering segments steering current to the positive output in response to a voltage present at the positive output [note that it is indicated that each of the current cell shown in fig. 1 comprises a control terminal that is used to control the differential input stage of the current cell, thereby in controlling the differential input stage of the cell the control circuit is reducing the variation in the voltage present at the summing node].

5. Regarding claim 3, Watson discloses a current steering DAC (figs. 1a – 2) wherein the control circuit comprises a second control circuit to reduce the variation of the voltage present at the summing node of each of the current steering segments steering current to the negative output in response to a voltage present at the negative output [note that it is indicated that each of the current cell shown in fig. 1 comprises a control terminal that is used to control the differential input stage of the current cell, thereby in controlling the differential input stage of the cell the control circuit is reducing the variation in the voltage present at the summing node](also, at the other end of the circuit a control terminal is also used in the transistor, for instance (d1 bar)].

6. Regarding claims 4, 33, Watson discloses a current steering DAC and method (figs. 1a – 2) wherein the control circuit [the control circuit as noted in col 1, lines 24 – 28 is at the input of the first transistor] comprises an operational amplifier (203, fig. 2) including first and second input terminals and an output terminal, wherein the output terminal is electrically connected to a substrate terminal of the differential transistor (fig. 2), that is electrically connected to the positive output, of each of the current steering segments (fig. 2)[note that fig. 2 is a representation of a current cell in which a control circuit is used at the input of the transistor]; a reference voltage source (Vbias2) electrically connected to the first input terminal of the operational amplifier (203); and a transistor (201) including a first terminal electrically connected to the second input terminal of the operational amplifier (203), a second terminal electrically connected to the positive output (fig. 2), a control terminal electrically connected to a constant-voltage terminal (note the constant voltage at the top of the upper transistor], and a substrate terminal electrically connected to the output terminal of the operational amplifier (fig. 2).

7. Regarding claim 5, Watson discloses a current steering DAC (figs. 1a – 2), wherein the transistor comprises fingers of substantially the same length and width as the differential transistors that are electrically connected to the positive output of the DAC (figs. 1a – 2).

8. Regarding claim 6, Watson discloses a current steering DAC (figs. 1a – 2) wherein the transistor is configured to have substantially the same drain current as the differential transistors that are electrically connected to the positive output of the DAC (figs. 1a – 2).

9. Regarding claim 7, Watson discloses a current steering DAC (figs. 1a – 2), wherein the first input terminal of the operational amplifier (203, fig. 2) comprises a positive input terminal of the operational amplifier, and the second input terminal of the operational amplifier comprises a negative input terminal of the operational amplifier (fig. 2).

10. Regarding claim 11, Watson discloses a current steering DAC (figs. 1a – 2) wherein said transistor comprises a field effect transistor (FET) (figs. 1a – 2).

11. Regarding claim 12, Watson discloses a current steering DAC (figs. 1a – 2), wherein the first terminal of the FET comprises a source terminal of the FET, the second terminal of the FET comprises a drain terminal of said FET, and the control terminal of the FET comprises a gate terminal of the FET (figs. 1a – 2).

12. Regarding claim 13, Watson discloses a current steering DAC (figs. 1a – 2), wherein the terminal comprises a ground terminal (106b, fig. 1a).

13. Regarding claim 14, Watson discloses a current steering DAC (figs. 1a – 2) wherein the control circuit [the control circuit as noted in col 1, lines 24 – 28 is at the I n put of the first transistor] comprises an operational amplifier (203, fig. 2) including first and second input terminals and an output terminal, wherein the output terminal is electrically connected to a substrate terminal of the differential transistor (fig. 2), that is electrically connected to the positive output, of each of the current steering segments (fig. 2)[note that fig. 2 is a representation of a current cell in which a control circuit is used at the input of the transistor]; a reference voltage source (Vbias2) electrically connected to the first input terminal of the operational amplifier (203); and a transistor

(201) including a first terminal electrically connected to the second input terminal of the operational amplifier (203), a second terminal electrically connected to the positive output (fig. 2), a control terminal electrically connected to a constant-voltage terminal (note the constant voltage at the top of the upper transistor], and a substrate terminal electrically connected to the output terminal of the operational amplifier (fig. 2).

14. Regarding claim 15, Watson discloses a current steering DAC (figs. 1a – 2), wherein the transistor comprises fingers of substantially the same length and width as the differential transistors that are electrically connected to the positive output of the DAC (figs. 1a – 2).

15. Regarding claim 15, Watson discloses a current steering DAC (figs. 1a – 2), wherein the transistor comprises fingers of substantially the same length and width as the differential transistors that are electrically connected to the positive output of the DAC (figs. 1a – 2).

16. Regarding claim 16, Watson discloses a current steering DAC (figs. 1a – 2) wherein the transistor is configured to have substantially the same drain current as the differential transistors that are electrically connected to the positive output of the DAC (figs. 1a – 2).

17. Regarding claims 17, 36, 37, Watson discloses a current steering DAC and method (figs. 1a – 2), wherein the first input terminal of the operational amplifier (203, fig. 2) comprises a positive input terminal of the operational amplifier, and the second input terminal of the operational amplifier comprises a negative input terminal of the operational amplifier (fig. 2).

18. Regarding claim 21, Watson discloses a current steering DAC (figs. 1a – 2) wherein the transistor comprises a field effect transistor (FET) (figs. 1a – 2).

19. Regarding claim 22, Watson discloses a current steering DAC (figs. 1a – 2), wherein the first terminal of the FET comprises a source terminal of the FET, the second terminal of the FET comprises a drain terminal of said FET, and the control terminal of the FET comprises a gate terminal of the FET (figs. 1a – 2).

20. Regarding claim 23, Watson discloses a current steering DAC (figs. 1a – 2), wherein the terminal comprises a ground terminal (106b, fig. 1a).

21. Regarding claim 25, 39, Watson discloses a current steering DAC and method (figs. 1a – 2) wherein each of the current steering segments comprises a current-setting transistor for setting the current through the corresponding current setting transistor (figs. 1a – 2).

22. Regarding claims 26, 39, Watson discloses a current steering DAC (figs. 1a – 2), wherein each of the current steering segments comprises a cascode transistor for setting a drain-to-source voltage of the corresponding current steering segment (figs. 1a – 2).

23. Regarding claim 38, Watson discloses a method (figs. 1a – 2) wherein controlling the threshold voltage on or more differential transistors electrically connected to a negative output comprised generating a differential voltage responsive to a difference between the voltage at the negative output and a substantially constant voltage and controlling the threshold voltage of one or more differential transistors electrically connected to the negative output using the differential voltage (figs. 1a – 2)

Claim Rejections - 35 USC § 103

24. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

25. Claims 27, 30, 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watson (US Patent Number 6,445,322) in view of the applicant's admitted prior art (APA).

26. Regarding claim 27, Watson discloses all the limitation as discussed above except a current steering DAC that comprises a thermometer code decoder to generate signals for controlling the current steering of each of the current steering segments in response to an input digital signal. However, the APA, in the same field of endeavor, discloses a current steering DAC that comprises a thermometer code decoder to generate signals for controlling the current steering of each of the current steering segments in response to an input digital signal (fig. 1). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was to couple the APA's current steering DAC that comprises a thermometer decoder in Watson's system in order to selectively steer current to either a positive output or negative out in the system.

27. Regarding claims 30, 35, both Watson and the APA does not explicitly discloses a method wherein the summing nodes comprises a comparing means that compares voltage at positive output with a substantially voltage. However, one skilled in the art

would understand that if one has to vary the voltage one has to a have a reference voltage of which a comparison has to be made. Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made that the combination of Watson and the APA would perform the same function as the same invention and would achieve the same end result.

Allowable Subject Matter

28. Claims 8 – 10, 18 – 20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

29. Reasons for allowing these claims will be provided in the next office action.

Conclusion

30. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

31. Tesch (US Patent Number 5,790,060) discloses a DAC having enhanced current steering and associated method.

32. Huang (US Patent Number 6,696,894) discloses an operational amplifier with independent input offset trim for high and low common mode input voltages.

33. Yao et al. (US Patent Number 09/749,976) discloses a current steering DAC and unit cell.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jean B Jeanglaude whose telephone number is 571-

272-1804. The examiner can normally be reached on Monday - Friday 7:30 A. M. - 5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jean Bruner Jeanglaude
Primary Examiner
October 28, 2004